

### In the Specification

**Please delete paragraph [0040], and replace it with the following paragraph:**

[0040] In accordance with the invention, as discussed above and further below, the vertical interfaces, i.e., resultant release structures, are located along the perimeter of the chip adjacent the crack stop, such that these release structures 22 face the dicing channels of the chip. During dicing, the material of the release structures 22 is loosely adhered to the walls of the crack stop such that it deflects any cracks from passing through the crack stop and instead diverts such cracks to travel along the crack stop, or is of a material having sufficient toughness, as discussed above, to absorb any cracks.

**Please delete paragraph [0044], and replace it with the following paragraph:**

[0044] The release layer 20 of the invention is then deposited over the structure shown in Fig. 2A in an amount sufficient to at least fill the release layer channel 55 on the outside perimeter 17 of crack stop 16 such that the vertical interface is formed along the perimeter of the chip adjacent the crack stop. In filling the release layer channel 55, release layer 20 is preferably deposited to a thickness ranging from about 50nm to about 1000nm. Again, an essential feature of the resultant vertical interface of the invention is that ~~is~~it be made of a release layer material that has a low adhesion interface for deflecting any possible cracks that may otherwise occur in the crack stop, and/or a material of sufficient toughness to absorb any generated crack energies. As such, the release layer may comprise any of the materials as discussed in detail above.

**Please delete paragraph [0051], and replace it with the following paragraph:**

[0051] Referring to Figs. 3E-F, the surface of the semiconductor structure is then planarized such that excess release layer 20 is removed in order to form release trench 26 that is substantially adjacent crack stop 16, therein being separated ~~by~~ from crack stop 16 by dielectric coating 19 on sidewalls of the release trench. Cap layer 40 is then deposited over the structure surface and planarized to provide the semiconductor structure with a substantially planar surface for further processing.

**Please delete paragraph [0060], and replace it with the following paragraph:**

In accordance with the invention, incorporating a hard mask into those processes making use of ultra-low-K dielectric materials may modify the above steps. In so doing, this hard mask protects the ultra-low-K dielectric materials during processing. Further, hard masks may be integrated into the above process steps for depositing the release layer material only into desired, select areas as may be required by the specific design structure. Another modification of the above approaches is to allow the release trenches be bounded ~~by~~ on each side by a metal line/via structure for allowing the dielectric material to be completely etched away without a potential problem of undercutting. Still another modification of the above processes is to allow the patterned block out resist, where used, to remain in place, deposit the release layer material and then simultaneously remove both the release layer and the patterned block out resist, such as by etching back. Still other modifications will be apparent to those of skill in the art.